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Product Features

- I²C control of all clocks and features
- IMI SSCG EMI reduction technology
- Dial-a-Skew™ feature
- 200 pS clock windows (like clocks)
- 200 pS clock Cycle to Cycle Jitter Performance
- 56 Pin SSOP package

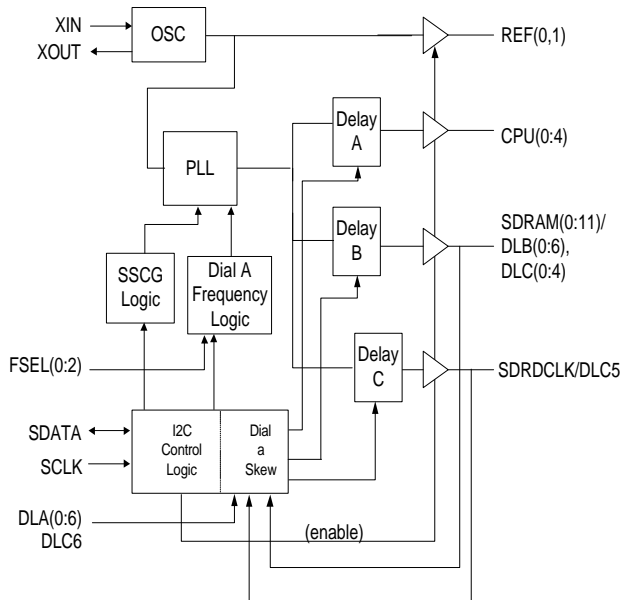
Product Description

The C5003 is a clock synthesizer which contains “state of the art” features, These include its Dial-a-Skew™ clock group offset control feature and I²C control of all major device features.. It contains a standard frequency table with 66.6 to 150 MHz output frequencies and is supplied in a 56 pin SSOP package

SEL2	SEL1	SEL0	CPU(0:4)	SDRAM(0:11),SDRDCLK	REF
0	0	0	Tri-State	Tri-State	Tri-State
0	0	1	XIN/2	XIN/4	XIN
0	1	0	66.6 MHz	66.6 MHz	14.318 MHz
0	1	1	133.3MHz	133.3MHz	14.318 MHz
1	0	0	140 MHz	140 MHz	14.318 MHz
1	0	1	150MHz	150MHz	14.318 MHz
1	1	0	125 MHz	125 MHz	14.318 MHz
1	1	1	100MHz	100MHz	14.318 MHz

Table 1

Block Diagram



Pin Configuration

N/C	1	56	VDD
REF0	2	55	CPU0
REF1	3	54	CPU1
VSS	4	53	VSS
XIN	5	52	VDD
XOUT	6	51	CPU2
VDD	7	50	CPU3
VSS	8	49	CPU4
DLA0	9	48	VSS
DLA1	10	47	VDD
DLA2	11	46	SDRAM0/DLB0
DLA3	12	45	SDRAM1/DLB1
DLA4	13	44	VSS
DLA5	14	43	SDRAM2/DLB2
DLA6	15	42	SDRAM3/DLB3
VDD	16	41	VDD
OE	17	40	SDRAM4/DLB4
FSEL0	18	39	SDRAM5/DLB5
FSEL1	19	38	VSS
FSEL2	20	37	SDRAM6/DLB6
VDD	21	36	SDRAM7/DLC0
VSS	22	35	VDD
VDD	23	34	SDRAM8/DLC1
SCLK	24	33	SDRAM9/DLC2
SDATA	25	32	VSS
VSS	26	31	SDRAM10/DLC3
DLC6	27	30	SDRAM11/DLC4
SDRDCLK/DLC5	28	29	VDD



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Pin Description

Pin	Name	PWR	I/O	Description
5	XIN	VDD	I	Oscillator Buffer Input. Connect to a crystal or to an external clock.
6	XOUT	VDD	O	Oscillator Buffer Output. Connect to a crystal. Do not connect when an external clock is applied at XIN.
55, 54, 51, 50, 49	CPU (0:4)	VDD	O	3.3 Volt Host Clock Outputs. See Frequency Table on page one of this data sheet.
36, 34, 33, 31, 30	SDRAM(7:11) /DLC(0:4)	VDD	I/O PD	Power-on Bi-directional Input / Output. At power-up, these pins are inputs. When the power supply voltage crosses the input threshold voltage, the logic level on the pin is latched into the DLC register and the pins then becomes a copy of the SDRAM clocks. See IMI application note AN-0021 and the Dial-an-Offset™ section of this data sheet.
46, 45, 43, 42, 40, 39, 37	SDRAM(0:6) /DLB(0:6)	VDD	I/O PD	Power-on Bi-directional Input / Output. At power-up, these pins are inputs. When the power supply voltage crosses the input threshold voltage, the logic level on the pin is latched into the DLB register and the pins then becomes a copy of the SDRAM clocks. See IMI application note AN-0021 and the Dial-an-Offset™ section of this data sheet.
28	SDRDCLK/ DLC5	VDD	I/O PD	Power-on Bi-directional Input / Output. At power-up, these pins are inputs. When the power supply voltage crosses the input threshold voltage, the logic level on the pin is latched into the DLC5 register bit and the pins then becomes a copy of the SDRAM clocks which has its own offset control. See IMI application note AN-0021.
27	DLC6	VDD	I PD	SDRDCLK most significant delay control bits. Only active when external hardware delay is selected.
2, 3	REF(0,1)	VDD	O	This pin is a 14.318MHz REF0 output clock.
9, 10, 11, 12, 13, 14, 15	DLA (0:6)	VDD	I PD	These pins (and their associated I ² C register counterpart's) permit adjusting the skew (offset) between the Devices PLL and CPU clock banks. See the "Dial-an-offset" section for functionality.
17	OE		I PU	Device output enable. When this pin is driven to a logic low level all output clocks are placed In a Tri-State mode. This function is an asynchronous event to any internal clocks.
18, 19, 20	FSEL (0:2)	VDD	I PU	Frequency Select Inputs. See Frequency Table on page one of this data sheet.
25	SDATA	VDD	I, PU	Serial I ² C Data Input. See IMI application note AN-0022.
24	SCLK	VDD	I, PU	Serial I ² C Clock Input. See IMI application note AN-0022.
7, 16, 21, 23, 29, 35, 41, 47, 52, 56	VDD	-	PWR	3.3V Common Power Supply
4, 8, 22, 26, 32, 38, 44, 48, 53	VSS	-	PWR	Common Ground

I = Input, O = Output, IO = Input and Output, PWR = Power, PU = Internal pull-up, PD = Internally pulled-down.



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Maximum Ratings

Maximum Input Voltage Relative to VSS: VSS - 0.3V
 Maximum Input Voltage Relative to VDD: VDD + 0.3V
 Storage Temperature: -65°C to + 150°C
 Operating Temperature: 0°C to +70°C
 Maximum ESD protection 2KV
 Maximum Power Supply: 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

$$VSS < (V_{in} \text{ or } V_{out}) < VDD$$

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL1	-	-	1.0	Vdc	Note 1
Input High Voltage	VIH1	2.0	-	-	Vdc	
Input Low Voltage	VIL2	-	-	1.0	Vdc	Note 2
Input High Voltage	VIH2	2.2	-	-	Vdc	
Input Low Current (@VIL = VSS)	IIL	4	9	-18	µA	For internal Pull up resistors, Notes 1, 2, 3, DL pins have pulldowns.
Input High Current (@VIL = VDD)	IIH	-5	0	5	µA	
Tri-State leakage Current	Ioz	-	-	10	µA	
VDD= 3.3V ±5%, TA = 0° to +70°C						

Note1: Applicable to input signals: FSEL(0:2), DLA(0:5), DLC6, OE

Note2: Applicable to Sdata, and Sclk.

Note3: Although internal pull-up resistors have a typical value of 450K, this value may vary between 300K and 750K. Internal Pull-down resistors are typically 375K in value, this value may vary between 250K and 800K.

2-Wire I²C Control Interface

The 2-wire control interface implements a read/write slave only interface according to Philips I²C specification. (See IMI Application Note [AN-0022](#)). Sub addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. 100 Kbits/s (standard mode) data transfer is supported.

The device will accept data written to the **D4** address and may read back from address **D5**. It will not respond to any other addresses, and previously set control registers are retained as long as power is maintained on the device.

Serial Control Registers

Following the acknowledge of the Address Byte, two additional bytes must be sent:

- 1) "**Command Code**" byte, and
- 2) "**Byte Count**" byte.

Although the data (bits) in the command code is considered "don't care"; it must be sent and will be acknowledged. The Byte count word should either be set to FF or the number of registers being written. A valid I²C stop condition will reset the devices internal byte counters. If more registers are written to than are specified in the byte count then the additional registers will not receive the data and the device will not acknowledge any operation for those bytes.



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After the Command Code and the Byte Count have been acknowledged, the sequence (Byte 0, Byte 1, and Byte 2) described below will be valid and acknowledged.

Byte 0: Clock Control Register

Bit	@Pup	Pin#	Description
7	0	12	Not Used
6	0	11	SSW1
5	0	10	SSW0
4	0	9	0=Spread Spectrum disabled 1=Spread Spectrum enabled
3	0	21	FSEL2
2	0	20	FSEL1
1	0	19	FSEL0
0	0	-	0= FSEL(0:2) and DL(A:C)(0:6) controlled by hardware pins. 1= FSEL(0:2) and DL(A:C)(0:6) controlled by I ² C Registers.

Byte 2: SDRAM Clock Register (1=Enable, 0=Disable)

Bit	@Pup	Pin#	Description
7	1	36	SDRAM7
6	1	37	SDRAM6
5	1	39	SDRAM5
4	1	40	SDRAM4
3	1	42	SDRAM3
2	1	43	SDRAM2
1	1	45	SDRAM1
0	1	46	SDRAM0

Byte 3: SDRAM Clock Register (1=Enable, 0=Disable)

Bit	@Pup	Pin #	Description
7	0	-	Not Used
6	0	-	Not Used
5	0	-	Not Used
4	1	28	SDRDCLK
3	1	30	SDRAM11
2	1	31	SDRAM10
1	1	33	SDRAM9
0	1	34	SDRAM8

Note 1: For enable control registers the Pin # column lists the relevant output pin number that is controlled. For skew control registers the Pin # column indicated the input pin function that the I²C bit is controlling when I²C Byte 0 Bit 0 is at a logic high state.

Note 2: The @Pup column gives the default register state at power up.

Note 3: Not Used I²C register bits listed as "Not Used" may be written to and read from (used as user R/W data storage).

Byte 1: REF and CPU Clock Register (1=Enable, 0=Disable)

Bit	@Pup	Pin#	Description
7	0	-	Reserved for IMI testing
6	1	49	CPU4
5	1	50	CPU3
4	1	52	CPU2
3	1	54	CPU1
2	1	55	CPU0
1	1	3	REF1
0	1	2	REF0

Byte 4: CPU Skew Register

Bit	@Pup	Pin#	Description
7	0	-	Reserved for IMI testing
6	0	15	DLA6
5	0	14	DLA5
4	0	13	DLA4
3	0	12	DLA3
2	0	11	DLA2
1	0	10	DLA1
0	0	9	DLA0

Byte 5: SDRAM Skew Register

Bit	@Pup	Pin#	Description
7	0	-	Reserved for IMI testing
6	0	37	DLB6
5	0	39	DLB5
4	0	40	DLB4
3	0	42	DLB3
2	0	43	DLB2
1	0	45	DLB1
0	0	46	DLB0

Byte 6: SDRDCLK Skew Register

Bit	@Pup	Pin#	Description
7	0	-	Reserved for IMI testing
6	0	27	DLC6
5	0	28	DLC5
4	0	30	DLC4
3	0	31	DLC3
2	0	33	DLC2
1	0	34	DLC1
0	0	36	DLC0



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Note 4: Reading FSEL(0:2), DLA(0:5) with Byte 0 Bit0 set to a logic 0 returns the state of the external pins. In the case of DLB and DLC registers, it returns the power up latched pin values. When Byte 0 Bit 0 is a logic 1, it returns the values stored within the internal I²C registers



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Spread Spectrum Clock Generation (SSCG)

Spread Spectrum is a modulation technique used to minimizing Electro-Magnetic Interference (EMI) radiation generated by repetitive digital signals. A clock presents the greatest EMI energy at the center frequency it is generating. Spread Spectrum distributes this energy over a specific and controlled frequency bandwidth therefore causing the average energy at any one point in this band to decrease in value. This technique is achieved by modulating the clock away from its resting frequency by a certain percentage (which also determines the amount of EMI reduction). In this device, Spread Spectrum is enabled by setting either I²B Byte 0 bit 4 to a 1 state. See IMI applications note [AN-0024](#) for a more in depth description of Spread spectrum modulation and see the I²C register section of this data sheet for the exact bit and byte functionality. The following table is a listing of the modes and percentages of Spread spectrum modulation that this device incorporates.

Spread Spectrum Selection Tables

Spread Code I ² C Byte 0		Spread	
Bit 6 (SSW1)	Bit 5 (SSW0)	Mode	Percentage
0	0	Down	+0% to -0.25%
0	1	Down	+0% to -0.50%
1	0	Down	+0% to -0.75%
1	1	Down	+0% to -1.00%

Dial-a-Skew™ Feature

The IMI I²C Dial-a-Skew™ feature is available in this device via both I²C control register bytes and external device pins. It allows the user to change three clock group timing relationships. The first adjustment is that between the CPU bank of output clocks and the internal PLL clock. The second is that between the SDRAM output clocks and the same internal PLL clock. The third is that between the SDRDCLK output clock and the same internal PLL clock. These adjustments operate independently of each other. See the block diagram on page 1 for a graphical description of these three skew control functions. The following tables describe the values of offset that may be attained by using this feature and how to select them. The timing values defined are measured at the 1.50-Volt rising edge point of the external clocks. These values are independent of any device inherent inner bank clock skewing and jitter that may be present. It is understood that the PLL's output clock (referred to as the "SOURCE" Clock) is at an absolute zero delay reference point in these values

As previously stated, this feature may be accessed in two ways.

1. The CPU, SDRDCLK and SDRAM offsets may be accessed with direct device pins 9 thru 15 and the power up bi-directional programmable pins on the SDRAM and SDRSCLK. To do this it is required that I²C Byte 0 bit 0 be set to a logic 0 condition.
2. By programming Byte 0 bit 0 to a logic 1. After this is done the values may be changed using the devices internal I²C registers.

By writing a logic 1 to I²C Byte 0 Bit 0 control may be changed to the internal I²C interface. When this is done, Bytes 4, 5 and 6, will then control the clock offset values. If the value in these I²C registers does not match the value that is contained in the external selection and power up latched pins when a change of offset source selection is made, output



clock glitching (cycles shorter than the selected frequency) may occur. To prevent this possible glitch condition the internal I²C control bytes should be set to the same data values as the external hardware values before Byte 0 Bit 0 is changed to a logic 1 condition. To retrieve the external and power up latched control bit states the user should read the respective delay registers when Byte 0 bit 0 = 0 and then write it back into the same bytes that it was read from.

Selecting new frequencies by changing the internal I²C clock delay register bits are guaranteed to produce glitch free transitions in all output clocks only when making incremental delay value steps. Wrap-around from 111 1111 to 000 0000 is not supported. When an incremental change is programmed, ALL clocks are stretched while in their low state to the next naturally occurring rising edge at the new delay timing settings.

SOURCE Clock to CPU, SDRAM and SDRDCLK Clock Offset Values

DL(A:C) 6-5-4-3-2-1-0	Programmed Frequency vs. Output Selection Code Skew			
	66, 100 and 133MHz	140Mhz	150MHz	125MHz
000 0000	0.000 ns	0.000 ns	0.000 ns	0.000 ns
000 0001	0.156 ns	0.156 ns	0.156 ns	0.156 ns
000 0010	0.312 ns	0.312 ns	0.312 ns	0.312 ns
000 0011	0.468 ns	0.468 ns	0.468 ns	0.468 ns
000 0100	0.624 ns	0.624 ns	0.624 ns	0.624 ns
000 0101	0.780 ns	0.780 ns	0.780 ns	0.780 ns
000 0110	0.936 ns	0.936 ns	0.936 ns	0.936 ns
000 0111	1.092 ns	1.092 ns	1.092 ns	1.092 ns
000 1000	1.250 ns	1.190 ns	1.111 ns	1.333 ns
000 1001				
000 1010				
000 1011				
000 1100				
000 1101				
000 1110				
000 1111				
001 0000	2.500 ns	2.380 ns	2.222 ns	2.666 ns
001 0001				
001 0010				
001 0011				
001 0100				
001 0101				
001 0110				
001 0111				
001 1000	3.750 ns	3.570 ns	3.333 ns	3.999 ns
001 1001				
001 1010				
001 1011				
001 1100				
001 1101				
001 1110				
001 1111				
010 0000	5.000 ns	4.760 ns	4.444 ns	5.332 ns
010 0001				
010 0010				
010 0011				
010 0100				



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010 0101				
010 0110				
010 0111				



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SOURCE Clock to CPU, SDRAM and SDRDCLK Clock Offset Values (Cont.)

DL(A:C) 6-5-4-3-2-1-0	Programmed Frequency vs. Output Selection Code Skew			
	66, 100 and 133MHz	140Mhz	150MHz	125MHz
010 1000	6.250 ns	5.950 ns	5.555 ns	6.665 ns
010 1001				
010 1010				
010 1011				
010 1100				
010 1101				
010 1110				
010 1111				
011 0000	7.500 ns	7.140 ns	6.666 ns	7.998 ns
011 0001				
011 0010				
011 0011				
011 0100				
011 0101				
011 0110				
011 0111				
011 1000	8.750 ns	8.330 ns	7.777 ns	9.331 ns
011 1001				
011 1010				
011 1011				
011 1100				
011 1101				
011 1110				
011 1111				
100 0000	10.000 ns	9.520 ns	8.888 ns	10.664 ns
100 0001				
100 0010				
100 0011				
100 0100				
100 0101				
100 0110				
100 0111				
100 1000	11.250 ns	10.710 ns	9.999 ns	11.997 ns
100 1001				
100 1010				
100 1011				
100 1100				
100 1101				
100 1110				
100 1111				
101 0000	12.50 ns	11.900 ns	11.110 ns	13.330 ns
101 0001				
101 0010				
101 0011				
101 0100				
101 0101				
101 0110				
101 0111				



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SOURCE Clock to CPU, SDRAM and SDRDCLK Clock Offset Values (Cont.)

DL(A:C) 6-5-4-3-2-1-0	Programmed Frequency vs. Output Selection Code Skew			
	66, 100 and 133MHz	140Mhz	150MHz	125MHz
101 1000	13.750 ns	13.090 ns	12.221 ns	14.663 ns
101 1001				
101 1010				
101 1011				
101 1100				
101 1101				
101 1110				
101 1111				
110 0000	15.00 ns	14.280 ns	13.332 ns	15.996 ns
110 0001				
110 0010				
110 0011				
110 0100				
110 0101				
110 0110				
110 0111				
110 1000	16.250 ns	15.470 ns	14.443 ns	17.329 ns
110 1001	16.406 ns	15.626 ns	14.559 ns	17.485 ns
110 1010	16.562 ns	15.782 ns	14.755 ns	17.641 ns
110 1011	16.716 ns	15.938 ns	14.911 ns	17.797 ns
110 1100	16.874 ns	16.094 ns	15.067 ns	17.953 ns
110 1101	17.030 ns	16.250 ns	15.223 ns	18.109 ns
110 1110	17.186 ns	16.406 ns	15.379 ns	18.265 ns
110 1111	17.342 ns	16.562 ns	15.535 ns	18.421 ns
111 0000	17.500 ns	16.666 ns	15.554 ns	18.662 ns
111 0001				
111 0010				
111 0011				
111 0100				
111 0101				
111 0110				
111 0111				
111 1000	18.750 ns	17.850 ns	16.665 ns	19.995 ns
111 1001	18.906 ns	18.006 ns	16.821 ns	20.151 ns
111 1010	19.062 ns	18.162 ns	16.677 ns	20.307 ns
110 1011	19.218 ns	18.318 ns	17.133 ns	20.463 ns
111 1100	19.374 ns	18.474 ns	17.289 ns	20.619 ns
111 1101	19.530 ns	18.630 ns	17.445 ns	20.775 ns
111 1110	19.686 ns	18.786 ns	17.601 ns	20.931 ns
111 1111	19.842 ns	18.942 ns	17.757 ns	21.087 ns

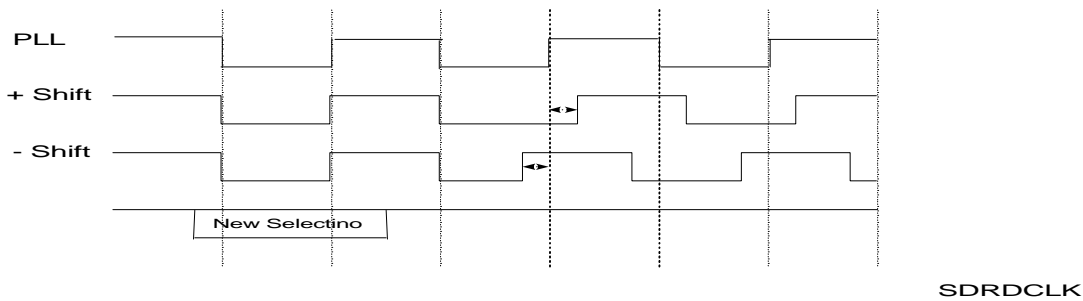
NOTE: To access this feature via the device's I²C control interface, I²C Byte 0 Bit 0 must be set to a logical 1 state. Otherwise these values will be programmed via the external DLA (0:5) hardware pins of the device. Times shown in tables are the time that the relevant clock lags (is delayed after) the internal PLL source.



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Synchronous Dial-a-Skew™ Switching

Logic down stream (loads) of the C5003 may be sensitive to the duty cycle changes that will occur if the Dial-a-Skew™ clock offset values are changed dynamically (in a running system). Included in the device is the necessary logic to insure minimum output clock period duty cycle distortions when this event occurs. This function is only supported when changes are being made using the device's I²C interface. The deviation of the affected output clocks duty cycle will only occur during a single low portion of one output clocks waveform. It is important that the application software that creates the I²C skew changing commands for the C5003's follow a strict rule of only changing these delays in single and minimal table adjacent timing steps. In order to move the delay 4 steps in time from a specific position four commands will be necessary. The following figure indicates (not to scale) how the output clocks respond to delay change commands in both the increase and decrease delay time scenario.



Internal logic is not guaranteed to create these synchronous steps if minimal skew changes are not programmed into the device via the I²C control interface.

Maximum Capacitive Loading Table

Clock Name	Max Load (in pF)
CPU (0:4)	30
SDRAM (0:11)	30
SDRDCLK	30
REF(0,1)	20



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AC Parameters

Symbol	Parameter	Specification		Units	Notes
		Min	Max		
TDC	Xin Duty Cycle	47.5	52.5	%	1, 4, 7
TPeriod	Xin period	69.8413	71.0	nS	1, 4, 7
VHIGH	Xin High Voltage	.7Vdd	Vdd	Volts	
VLOW	Xin Low Voltage	0	.3Vdd	Volts	
Tr / Tf	Xin rise and fall times	-	10.0	nS	3
TCCJ	Xin Cycle to Cycle Jitter	-	500	pS	2, 4, 5
TDC	CPU(0:4) Duty Cycle	45	55	%	1, 2, 4
Tr / Tf	CPU(0:4) rise and fall times	0.4	1.6	nS	2, 3
TSKEW	Any CPU clock to any CPU clock Skew	-	±200	pS	2, 6, 5
TCCJ	CPU(0:4) Cycle to Cycle Jitter	-	200	pS	2, 4, 5
Zout	CPU(0:4) buffer output Impedance			Ohms	
TDC	REF(0:1) Duty Cycle	45	55	%	1, 2, 4
Tr / Tf	REF(0:1) rise and fall times	1.0	4.0	nS	2, 3
TCCJ	REF(0:1) Cycle to Cycle Jitter	-	1000	pS	2, 4, 5
Zout	REF(0:1) buffer output Impedance			Ohms	
TDC	SDRAM(0:11) , SDRDCLK Duty Cycle	45	55	%	1, 2, 4
Tr / Tf	SDRAM(0:11) , SDRDCLK rise and fall times	0.4	1.6	nS	2, 3
TSKEW	Any SDRAM clock to any SDRAM clock Skew	-	±200	pS	2, 6, 5
TCCJ	SDRAM(0:11) , SDRDCLK Cycle to Cycle Jitter	-	200	pS	2, 6, 5
Zout	SDRAM(0:11) buffer output Impedance			Ohms	
Zout	SDRDCLK buffer output Impedance			Ohms	
tstable	All clock Stabilization from power-up	-	3	mS	6

Note 1: This parameter is measured as an average over 1uS duration, with a center frequency of 14.31818MHz

Note 2: All outputs loaded as per table below.

Note 3: Probes are placed on the pins, and measurements are acquired between 0.4V and 2.4V (see test conditions section of this data sheet)

Note 4: Probes are placed on the pins, and measurements are acquired at 1.5V. (See test conditions section of this data sheet)

Note 5: This measurement is applicable with Spread ON or spread OFF

Note 6: The time specified is measured from when VDD reaches its supply rail (3.3V) till the frequency output is stable and operating within the data sheet specifications.

Note 7: When Xin is driven from and external clock source.

Bank to Bank Clock Skew

This device has 3 Dial-a-Skew™ registers. With these registers 2 major banks (the CPU clocks bank and the SDRAM bank) can have their timing adjusted with respect to each other. When the offset that is programmed into these banks is equal they act as a single bank. In this configuration the CPU and SDRAM inter clock skew is defined by the specification of the AC parameters table (a ± 200pSec position window). This figure describes the skewing of these clocks over data sheet voltage, temperature and any device manufacturing variations.

When the clocks are offset at different amounts (from the internal reference clock) an additional factor enters into the skewing between these clocks. It is created by the difference in delay they encounter within the part. This additional figure of timing ambiguity adds to the previously stated ±200pSec position accuracy. Its value can be determined from the clock bank offset tables.



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AC Component Parameters (VDD = 3.3V ±5%, TA = 0°C to +70°C)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Dynamic Supply Current ¹	I _{dd3.3V}	-	250	TBD	mA	CPU, SDRAM at 66 MHz,
		-	380	TBD	mA	CPU, SDRAM at 100 MHz
		-	480	TBD	mA	CPU, SDRAM at 133 MHz
Input pin capacitance	C _{in}	-	-	5	pF	
Output pin capacitance	C _{out}	-	-	6	pF	
Pin Inductance	L _{pin}	-	-	7	nH	
Crystal pin capacitance	C _{xtal}	30	36	42	pF	Measured from the Xin or Xout Pin to Ground.

Note1: All outputs loaded as per maximum capacitive load table.

Output Buffer DC Characteristics

SDRAM(0:11), SDRDCLK, CPU(0:4)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH ₁	22	-	-	mA	V _{out} = VDD-0.5V
Pull-Up Current	IOH ₂	63	-	-	mA	V _{out} = VDD/2
Pull-Down Current	IOL ₁	17.7	-	-	mA	V _{out} = 0.4 V
Pull-Down Current	IOL ₂	55	-	-	mA	V _{out} = 1.2V

REF (0,1)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH ₁	6.1	-	-	mA	V _{out} = VDD-0.5V
Pull-Up Current	IOH ₂	17.7	-	-	mA	V _{out} = VDD/2
Pull-Down Current	IOL ₁	5.9	-	-	mA	V _{out} = 0.4 V
Pull-Down Current	IOL ₂	21	-	-	mA	V _{out} = VDD/2

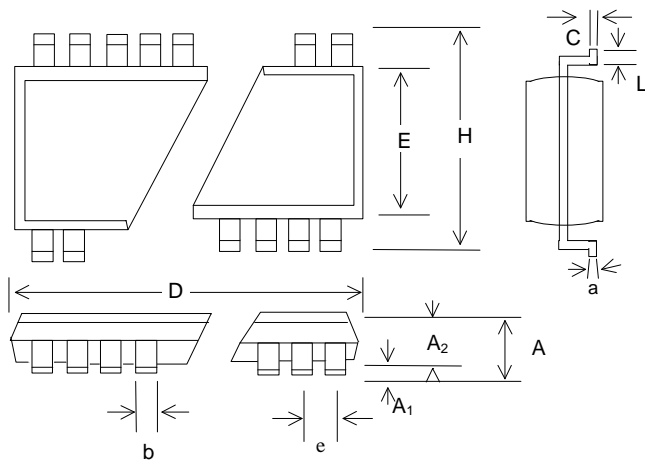


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Advanced Feature Clock Generator for PPC Products

Preliminary

Package Drawing and Dimensions



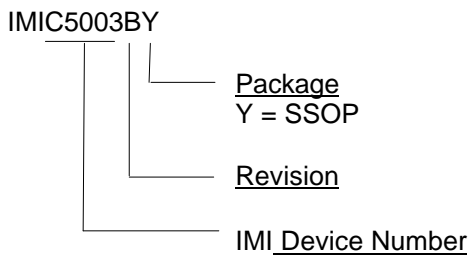
56 Pin SSOP Outline Dimensions

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A ₁	0.008	0.012	0.016	0.203	0.305	0.406
A ₂	0.088	-	0.092	2.24	-	2.34
B	0.008	-	0.0135	0.203	-	0.343
C	0.005	-	0.010	0.127	-	0.254
D	0.720	0.725	0.730	18.29	18.42	18.54
E	0.291	0.295	0.299	7.39	7.49	7.60
e	0.025 BSC			0.635 BSC		
H	0.395	-	0.420	10.03	-	10.67
L	0.020	-	0.040	0.508	-	1.016
a	0°	-	8°	0°	-	8°

Ordering Information

Part Number	Package Type	Production Flow
C5003BY	56 Pin SSOP	Commercial, 0°C to +70°C

Marking: Example: IMI
C5003BY
Date Code, Lot #





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Advanced Feature Clock Generator for PPC Products

Preliminary

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